REMARKS

Applicants have amended claims 2, 3, 5, 7 16, 17, 19, 21, 31 and 32 and cancelled claims 1, 4, 6, 8-15, 18, 20, 22-30 and 33-36 from further consideration in this application. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications

The Examiner rejected claims 2, 3, 5, 7, 16, 17, 19, 21 and 31-32 under 35 U.S.C. § 102(b) as allegedly being clearly anticipated by Blaner et al. "An Embedded Power PC™ SOC for Test and Measurement Applications", IEEE 2000, hereafter Blaner.

Applicants respectfully traverse the § 102 rejections with the following arguments.

35 U.S.C. § 102(b)

The Examiner rejected claims 2, 3, 5, 7, 16, 17, 19, 21 and 31-32 under 35 U.S.C. § 102(b) as allegedly being clearly anticipated by Blaner et al. "An Embedded Power PC™ SOC for Test and Measurement Applications", IEEE 2000, hereafter Blaner.

As to claim 31, the Examiner stated the reference discloses "loading into said memory unit, code representing (i) an external memory model connected to a simulated external memory mapped test device and to said simulated memory controller, (ii) one or more first external I/O driver models connected between said simulated I/O cores and said simulated external memory mapped test device and (iii) one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller, said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case, all said connections of (i), (ii) and (iii) by corresponding simulated I/O buses" referencing "page 208, section IV-E, 'memory mapped external device') Figure 1, OPN, UART, GPIB)."

Applicants respectfully contend that Blaner does not anticipate claim 31, because Blaner does not teach each and every feature of claim 31.

In a first example, Blaner does not teach. "one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller."

In a second example, Blaner does not teach "one or more first external I/O driver models connected between said simulated I/O cores and said simulated external memory mapped test device."

In a third example Blaner does not teach "said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case."

(1) Applicants respectfully point out that section IV-E of Blaner states only "a memory-mapped external device containing software readable and writable registers that appear as wires in the testbench is connected to the external bus." Applicants find no mention of "a simulated switch" no less any connections to the switch.

(2) Applicants have attached a declaration signed by Robert J. Devins an inventor of the present invention and an author of the referenced Blaner IEEE paper stating in part "the referenced IEEE paper 'An embedded Power PC SOC for Test and Measurement Applicants' does not teach nor was intended to teach an EMMTD having a simulated switch. The simulated external memory mapped test device of the referenced IEEE paper does not contain any means for selecting models to connect between the EMMTD and the SOC."

(3) Applicants respectfully point out that the "OPN, UART, GPIB" cited by the Examiner are in the SOC of Figure 1, which makes them the "simulated I/O cores" not the" first external I/O driver models" or "second external I/O driver models" of Applicants claim 31.

Based on the preceding arguments, Applicants respectfully maintain that Blaner does not anticipate claim 31, and that claim 31 is in condition for allowance. Since claims 2, 3, 5, 7 and 21 depend from claim 31, Applicants contend that claims 2, 3, 5, 7 and 21 are likewise in condition for allowance.

Applicants respectfully contend the Arguments presented *supra* with respect to claim 32 are applicable to claim 32 and Applicants respectfully maintain that Blaner does not anticipate claim 32, and that claim 32 is in condition for allowance. Since claims 16, 17 and 19 depend

from claim 32, Applicants contend that claims 16, 17 and 19 are likewise in condition for allowance.

As to claims 2, 7 and 19, Applicants contend that Blaner does not teach "wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective second external I/O driver model of said second external I/O driver models."

Applicants respectfully point out, Blaner teaches only a single "external memory mapped test device" not "a plurality of simulated external memory mapped test device modules" as claims 2, 7 and 19 requires. Further, Blaner does not teach "each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch" or even a switch, as Applicants claims 2, 7 and 19 requires. Applicants respectfully maintain that Blaner does not anticipate claims 2, 7 and 19, and that claims 2, 7 and 19 are in condition for allowance.

As to claim 19, Blaner does not teach "executing said instructions, further causes said computer to connect each portion of said simulated switch to one second external I/O driver model of said one or more I/O driver models using address information programmed into its corresponding simulated address register."

Applicants respectfully point out that Blaner does not teach a "switch" nor does Blaner teach "using address information programmed into its corresponding simulated address register"

to "connect each portion of said simulated switch to one second external I/O driver model of said one or more I/O driver models." As argued *supra*, with respect o claim 32, Blaner does not teach a :switch." As to the registers, Blaner only teaches the EMMTD registers "appear a wires in the testbench." There is no other teaching about the registers. Applicants respectfully maintain that Blaner does not anticipate claim 19, and that claim 19 is in condition for allowance.

Attachments:

Declaration of Robert J. Devins.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456 (IBM).

Respectfully submitted,
FOR:
Devins et al.

BY:

/ Anthony M. Palagonia /
Anthony M. Palagonia
Registration No.: 41,237

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Schmeiser, Olsen & Watts
22 Century Hill Drive, Suite 302
Latham, New York 12110
(518) 220-1850 Telephone
(518) 220-1857 Facsimile

Agent Direct Dial Number: (802)-899-5460